CLAIMS

What is claimed is:

1. A method comprising:

physically storing a plurality of images in a plurality of physical address space portions while logically storing the plurality of images in a common virtual address space, wherein at least a portion of the plurality of images logically stored in the common virtual address space are overlapping;

receiving a request to access one of the plurality of images;

translating a logical entry point for the image requested to be accessed from a virtual address in the common virtual address space to a physical address in the physical address space portion in which the image is stored to access the image.

2. The method of claim 1, further comprising:

building a virtual translation table containing entries corresponding to the plurality of images, each entry to map a virtual location in the common virtual address space at which an image is logically stored to a physical location in the physical address space at which the image is physically stored;

identifying an entry in the virtual translation table corresponding to the image requested to be accessed, the entry including information for mapping the logical entry point of the image from the virtual location in the common virtual address space to the physical location in the physical address space instance.

programming a hardware component to automatically map an access request of the image from the virtual location in the common virtual address space to the physical location in the physical address space instance using information contained in the entry.

3. The method of claim 2, wherein the hardware component comprises a processor.

4. The method of claim 3, wherein the processor includes a plurality of translation registers, the method further comprising:

dynamically programming a translation register to automatically effect a mapping of the access request.

5. The method of claim 2, further comprising:

loading a set of the plurality of images into the same physical address space portion; and

creating an entry in the virtual translation table for each of the images that are loaded, the entry defining a logical entry point for the image comprising a virtual address in the virtual address space that is mapped to a physical address comprising a physical entry point at which the image is accessed.

6. The method of claim 2, wherein the operation of programming the hardware component to automatically map the access request is performed by firmware.

7. The method of claim 1, wherein the plurality of images comprise option ROM (read-only memory) images.

8. The method of claim 7, wherein the option ROM images include at least one option ROM image stored on an ISA (industry standard architecture) legacy card.

9. The method of claim 7, wherein the option ROM images include at least one option ROM image stored on an PCI (peripheral component interface) card.

10. The method of claim 7, wherein the common virtual address space includes virtual addresses spanning C- and D-segments defined by the PC-AT (personal computer-advanced technology) architecture for storing option ROM images.

11. The method of claim 10, wherein at least one of the physical address space portions comprises an instance of the C- and D-segments.

12. A method, comprising:

shadowing option ROM images into a physical address space of system memory for a computer system, each option ROM image that is shadowed having a respective physical entry point and being shadowed from an option ROM hosted by a respective peripheral card ;

logically storing the option ROM images that are shadowed in a common virtual address space, wherein at least a portion of the option ROM images in the common virtual address space are overlapping; and

mapping a virtual address comprising a logical entry point to each option ROM image to a corresponding physical address comprising the physical entry point for that option ROM image.

13. The method of claim 12, wherein at least a portion of the option ROM images are shadowed into a physical address space instance having a size equivalent to a size of the common virtual address space.

14. The method of claim 13, wherein groups of option ROM images are shadowed into a respective physical address space instances having a size equivalent to the size of the common virtual address space.

15. The method of claim 12, wherein the common virtual address space includes virtual addresses spanning C- and D-segments defined by the PC-AT (personal computer-advanced technology) architecture for storing option ROM images.

16. The method of claim 12, further comprising:

building a virtual translation table containing entries corresponding to the plurality of option ROM images, the entries including information to map a logical entry point for each option ROM image to its corresponding physical entry point.

17. The method of claim 16, further comprising:

receiving an access request to a peripheral card;

identifying an entry in the virtual translation table corresponding to the peripheral card requested to be accessed, the entry including information for mapping the logical entry point of the image from the virtual address in the common virtual address space to the physical address in the physical address space instance.

programming a hardware component to automatically map an access request of the image from the virtual address in the common virtual address space to the physical address in the physical address space instance using information contained in the entry.

18. The method of claim 12, wherein the option ROM images include at least one option ROM image stored on an ISA (industry standard architecture) legacy card.

19. The method of claim 12, further comprising:

performing the mapping such that it appears to system hardware that there are never any overlapping option ROM images in the common virtual address space.

20. An article of manufacture, comprising a machine-accessible medium having instructions stored thereon, which when executed perform operations including:

shadowing a plurality of option ROM images into portions of a physical address space; and

mapping a physical entry point for each of the plurality of option ROM images to a logical entry point corresponding to a virtual address in a common virtual address space such that the plurality of option ROM images logically reside in the common virtual address space,

wherein an aggregated size of the plurality of option ROM images is greater than a size of the common virtual address space.

21. The article of manufacture of claim 20, wherein the machine-accessible medium includes further instructions to perform the operation of:

programming a hardware component to automatically effectuate a mapping for an individual option ROM image in response to a request to access that option ROM image,

wherein the request to access the option ROM image references the logical entry point for the option ROM image.

22. The article of manufacture of claim 21, wherein the hardware component is a processor.

23. The article of manufacture of claim 21, wherein the machine-accessible medium includes further instructions to perform the operation of:

building a virtual translation table containing entries corresponding to the plurality of option ROM images, including entries to map a logical entry point for each option ROM image to its corresponding physical entry point; and

programming the hardware component using information contained in the entry corresponding to the option ROM image for which access is requested.

24. The article of manufacture of claim 20, wherein the common virtual address space includes virtual addresses spanning C- and D-segments defined by the PC-AT (personal computer-advanced technology) architecture for storing option ROM images.

25. The article of manufacture of claim 21, wherein the option ROM image physically occupies multiple physical pages and logically occupies multiple virtual pages, the machine-accessible medium including further instructions to perform the operation of:

detecting a page fault in response to an attempt to access a second virtual page at which a portion of the option ROM image is logically resides; and

programming a translation register to effect an address translation from the second virtual page to a second physical page at which a portion of the option ROM is shadowed.

26. A system, comprising:

a processor;

system memory, operatively coupled to the processor and defining a physical address space;

a plurality of expansion slots, operatively coupled to the processor, each expansion slot configured to accept an add-on peripheral card; and

a firmware storage device, having firmware instructions stored thereon, which when executed by one of the processor or a virtual machine hosted by the processor perform operations, comprising:

shadowing a plurality of option ROM images into portions of the physical address space, the option ROM images being stored on respective add-on peripheral cards that were installed in at least a portion of the plurality of expansion slots; and

for each of the plurality of option ROM images,

mapping a physical page or pages at which that option ROM image is shadowed to a corresponding virtual page or pages in a common virtual address space such that the plurality of option ROM images logically reside in the common virtual address space,

wherein a portion of the option ROM images are logically stored on overlapping virtual pages.

27. The system of claim 26, wherein the firmware storage device comprises a flash device.

28. The system of claim 26, wherein the processor comprises an Intel IA-64 architecture processor.

29. The system of claim 28, wherein the firmware instructions perform the further operations of:

detecting a request to access an option ROM image at its logical location ;

programming a translation register to effect an address translation from a virtual page at which the option ROM image is logically stored to a physical page at which the option ROM image is shadowed.

30. The system of claim 29, wherein the option ROM image physically occupies multiple physical pages and logically occupies multiple virtual pages, the firmware instructions to perform the further operations of:

detecting a page fault in response to an attempt to access a second virtual page at which a portion of the option ROM image is logically resides; and

programming a translation register to effect an address translation from the second virtual page to a second physical page at which a portion of the option ROM is shadowed.